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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

MEYER, DAVID C

ART UNIT	PAPER NUMBER
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2878

DATE MAILED: 01/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/976,511

Applicant(s)

WU ET AL.

Examiner

David C Meyer

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 October 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 8-11, 14-16, 19-21 and 23-25 is/are rejected.
- 7) ☒ Claim(s) 5-7, 12, 13, 17, 18 and 22 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claim 16 is objected to because of the following informalities: line 1 contains the phrase "A method apparatus". Claim 16 is obviously a method claim and should be reworded to reflect this. The word "apparatus" should be removed from line 1, and the phrase "the steps of" should be inserted after the word "comprising" in line 6.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-4, 8-11, 16, 21, and 23 are rejected under U.S.C. 103(a) as being unpatentable over Geller (US Patent 5,202,553) in view of Lim (US Patent 5,329,115) and in further view of Lemon et al (US Patent 5,953,690).

Regarding claim 1, Geller discloses a transimpedance amplifier comprising amplifiers 14 and 16 and coupled to photodiode 12; a current to voltage circuit comprising a resistor 32 and a current mirror 39 which generates a voltage signal based on the strength of a detected optical signal; and a comparator circuit 36 comprising a comparator U1A which is coupled to the current to voltage circuit and which provides a signal that reflects the strength of the detected optical signal (Fig. 5 and column 3, line 21 to column 5, line 16). Geller does not disclose that the transimpedance amplifier is AC coupled to the photodiode. Lim teaches an optical receiver circuit wherein a transimpedance amplifier 48 is AC coupled to a photodetector 32 (Fig. 2). Lim also teaches that AC coupling of a current signal to a transimpedance amplifier is required where a small signal may have a varying or large DC component that must be subtracted from the current signal before it can be accurately amplified (column 1, lines 33-37). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Geller by AC coupling the transimpedance amplifier to the photodetector in order to facilitate more accurate current signal amplification in the face of a varying DC signal.

Geller also does not disclose that the current to voltage circuit and comparator comprise a loss of signal (LOS) circuit. However, Geller does disclose all the elements of the claimed LOS circuit. Furthermore, because the signal that the comparator generates reflects the strength of the detected optical signal it could be used to indicate a loss of signal strength. Lemon et al teaches that a comparator in an opto-electronic receiver may be used to generate a loss of signal signal. Lemon et al discloses an opto-electronic receiver comprising a loss of signal alarm. The loss of signal alarm comprises a comparator 624 which compares the strength of a detected optical signal to a reference voltage (generated at 622) and generates a loss of signal signal when the

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detected signal strength is lower than a predetermined voltage (column 13, line 54 to column 14, line 38). It would have been obvious to one of ordinary skill in the art at the time of invention to use the current to voltage circuit and comparator disclosed in Geller to generate a voltage signal indicative of a LOS because it would facilitate a correction function in the event of a loss of signal.

Claims 8, 11, and 21 contain substantially the same subject matter as recited in claim 1. As such, the same rejection that applies to claim 1 applies equally to claims 8, 11, and 21.

Regarding claim 2, the current to voltage circuit Geller discloses comprises a current mirror 39 which receives a DC current and provides a DC voltage signal to comparator U1A (Fig. 5).

Regarding claim 3, the current mirror Geller discloses comprises transistors Q8 and Q9 which receive a signal from sense resistor 32. The resistor could provide a substrate drive signal.

Regarding claim 4, the resistor 32 Geller discloses could be used to provide process and temperature information.

Claim 23 contains substantially the same subject matter as recited in claim 4. As such the same rejection that applies to claim 4 applies equally to claim 21.

Regarding claim 9, Geller discloses a transimpedance amplifier comprising amplifiers 14 and 16.

Regarding claim 10, the voltage signal produced by the resistor, capacitor, and current mirror is compared to a reference voltage V_R by comparator U1A (column 3, lines 52-57).

Regarding claim 16, Geller discloses elements that perform all of the steps recited in method claim 16. Geller discloses a photodetector 12 which generates a DC signal responsive to

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an optical signal; a current to voltage converter circuit comprising resistor 32, capacitor 34, and a current mirror 39 and which is coupled to the photodetector and which generates a voltage signal in response to the DC signal; a comparator circuit 36 which receives the voltage signal and which generates a voltage signal corresponding to the strength of the initial optical signal. This voltage signal constitutes a loss of signal signal.

5. Claims 14, 15, 24, and 25 are rejected under U.S.C. 103(a) as applied to claim 11 above in further view of Kollanyi (US Patent 4,893,002).

Regarding claim 14, Geller does not disclose a translator circuit which adjusts the signal generated by the comparator circuit. Kollanyi teaches as part of a loss of optical input circuit a comparator circuit comprising transistors 20 and 25. The comparator circuit forwards a voltage signal to an alarm circuit. The alarm circuit provides a logic signal corresponding to a loss of signal. The alarm circuit comprises a translator circuit and the logic signal constitutes an adjusted loss of signal signal (column 3, line 48 to column 4, line 11). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Geller by including a translator circuit to generate an adjusted LOS signal reflecting the strength of the original detected optical signal in order to facilitate an appropriate response function when a loss of signal strength is detected.

Claim 24 contains substantially similar subject matter as recited in claim 14. As such, the same rejection that applies to claim 14 applies equally to claim 24.

Regarding claim 15, Geller discloses a reference voltage signal V_R . While Geller does not disclose specific circuitry for generating the voltage signal, such circuitry is an inherent part of

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Geller's invention. Geller also discloses a comparator 36 that compares the detected voltage signal to the reference voltage signal.

Claim 25 contains substantially similar subject matter as recited in claim 15. As such, the same rejection that applies to claim 15 applies equally to claim 25.

6. Claims 19 and 20 are rejected under U.S.C. 103(a) as applied to claim 16 above in further view of Kollanyi (US Patent 4,893,002).

Regarding claim 19, Geller does not disclose the steps of coupling a translator circuit to the comparator circuit, receiving the LOS signal by the translator circuit from the comparator circuit, and generating an adjusted LOS signal. Kollanyi teaches elements that perform the steps recited in claim 19. Specifically, Kollanyi discloses an alarm circuit that produces a logic signal in response to a LOS signal generated by a comparator circuit. The alarm circuit constitutes a translator circuit and the logic signal corresponds to an adjusted LOS signal (column 3, line 48 to column 4, line 11). It would have been obvious to one of ordinary skill in the art to modify the method for generating a LOS signal disclosed by Geller by coupling a translator circuit to the comparator circuit and subsequently providing an adjusted LOS signal using that translator circuit in order to facilitate an appropriate response function when a loss of signal strength is detected.

Regarding claim 20, Geller does not disclose the step of providing a reference voltage generator circuit, but he does disclose a reference voltage which is used in the step of comparing a voltage signal with a reference voltage signal to generate a LOS signal. The step of providing the circuitry is an inherent aspect of Geller's invention.

Allowable Subject Matter

7. Claims 5-7, 12-13, 17-18, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 5-7, the prior art of record does not disclose or make obvious the invention as claimed, specifically wherein the temperature sensor comprises a resistor and a transistor.

Regarding claims 12-13, 17-18, and 22 the prior art of record does not disclose or make obvious the invention as claimed, specifically wherein a voltage buffer circuit is coupled to the current mirror and the voltage buffer circuit receives an intermediate voltage signal and generates a voltage signal.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Roberts (US Patent 5,286,969) discloses an apparatus for measuring optical power in an optical receiver.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David C Meyer whose telephone number is 703-305-7955. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on 703-308-4852. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0935.

DCM

January 13, 2003



DAVID PORTA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800